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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,271	01/25/2001	Tsukasa Yajima	PNET.009D	3802

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EXAMINER	
MAI, ANH D	
ART UNIT	**PAPER NUMBER**
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/768,271	YAJIMA, TSUKASA	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,7,9,11-13 and 15-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,7,9,11-13 and 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 13, 2006 is acknowledged.

Status of the Claims

2. Amendment filed November 13, 2006 is acknowledged. Claims 6, 11 and 16 have been amended. Claims 6, 7, 9, 11-13 and 15-19 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 6, 7, 9, 11-13 and 15-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "a protective layer formed directly on said field oxide to prevent overetching of said field oxide, said protective layer being a conductive layer, having side surfaces thereof over said field oxide and **having substantially uniform thickness**" (as recited in amended claims 1, 11 and 16) in the application as filed.

Note that, the "protective" layer 12, is formed by planarizing (CMP) the polysilicon layer 11 which is formed on the field oxide 34, Fig. 1d-1e. There is no evidence from the specification that layer 12 has uniform thickness or substantially uniform thickness, since there are too many variable, the surface of the field oxide 34, changing the profile of oxidation masking layer 33, the etch that removes layer 32 and 33, etc.,. Also, the specification is completely silence with respect to the uniform thickness of layer 12.

Applicant must provide support for or cancel the new matter.

This is a repeated rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 6, 7, 9, 11-13 and 15-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoo et al. (U.S. Patent No. 5,605,853) of record.

With respect to claim 6, Yoo teaches a semiconductor device as claimed including:

first (16) and second (16) gates formed on an active regions of a substrate (10), the first and second gates (16) each consisting of a refractory metal layer (28) on a polysilicon layer (16) and each having side surfaces;

a field oxide (12) formed on the substrate (10) between the first and second gate (16);

protective layer (21) formed directly on the field oxide (12) to prevent overetching of the field oxide, the protective layer (21) being a conductive layer, and being formed so as not to be on edges of the field oxide (12) and as having substantially uniform thickness;

sidewall spacers (20) of silicon oxide film formed on the side surfaces of the first and second (16) gates; and

an insulating layer (38), a contact hole, and a connecting wire (40) formed above the surface of the substrate (10). (See Fig. 7).

Since the protective layer (21) of Yoo is formed directly on the field oxide, thus the protective layer (21) is fully capable of preventing overetching of the field oxide (12).

With respect to claim 11, Yoo teaches a semiconductor device as claimed including:

a gate (16) formed on an active region of a substrate (10), gate (16) having side surfaces;

a field oxide (12) formed on the substrate (10) adjacent the active region;

a protective layer (21) formed directly on the field oxide (12) to prevent overetching of the field oxide, the protective layer (21) being a conductive layer, and being formed so as not to be on edges of the field oxide (12) and as having substantially uniform thickness;

sidewall spacers (20) formed on the side surfaces of gate (16); and

an insulating layer (38), a contact hole, and a connecting wire (40) formed above the surface of the substrate (1),

the protective layer (21) being formed on the field oxide only. (See Fig. 7).

Since the protective layer (21) of Yoo is formed directly on the field oxide, thus the protective layer (21) is fully capable of preventing overetching of the field oxide (12).

With respect to claim 16, as best understood by the examiner, Yoo teaches a semiconductor device as claimed including:

a gate (16) formed on an active region of a substrate (10), the gate (16) consisting of a refractory metal layer (24) on a polysilicon layer and having side surfaces;

a field oxide (12) formed on the substrate (10) adjacent the active region;

a protective layer (21) formed directly on the field oxide (12) to prevent overetching of the field oxide, the protective layer (21) being a conductive layer, and being formed so as not to be on edges of the field oxide (12) and as having substantially uniform thickness;

sidewall spacers (20) of silicon oxide film formed on the side surfaces of the gate (16); and

an insulating layer (38), a contact hole, and a connecting wire (40) formed above the surface of the substrate (1),

the protective layer (21) being formed on the field oxide (12) only. (See Fig. 7).

Since the protective layer (21) of Yoo is formed directly on the field oxide, thus the protective layer (21) is fully capable of preventing overetching of the field oxide (12).

With respect to claims 7, 12 and 17 the protective layer (21) of Yoo is a polysilicon layer.

With respect to claims 9, 13 and 18, the first and second gates (16) of Yoo are a MOSFET gates.

With respect to claims 15 and 19, the semiconductor device of Yoo further comprising an additional gate (16) formed on the substrate (10), the field oxide (12) being formed on the substrate (10) between the gate (16) and the additional gate (16).

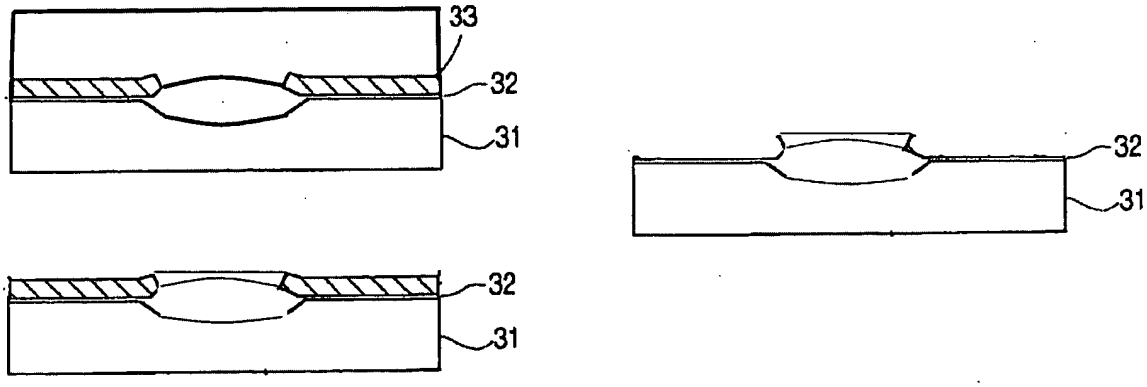
Response to Arguments

5. Applicant's arguments filed November 13, 2006 have been fully considered but they are not persuasive.

Claims Rejected under 35 U.S.C. 112, first paragraph:

Regarding the new matter: the protective layer "as having substantially uniform thickness", Applicant asserts: since the protective layer of the present application *is planarized*, the protective layer should be understood as having substantially uniform thickness, *although not exactly*.

The "although not exactly" is the most correct.



The convex nature of the field oxide are well known in the art and has been recognized by the Applicant. As illustrated above, after the planarization, the middle portion of the protective layer should be thinner that the rest of the protective layer on the field oxide, regardless of the protective has been formed at the edge or not.

Since the specification is completely silent regarding the uniform nature of the protective layer as originally file, any subsequent amendment that adds the unsupported subject matter is considered to be new matter.

Planarizing the polysilicon layer 11 on the field oxide 34 only flattens the surface, not forming an uniform thickness.

The rejection is therefore, maintained.

Claims rejected under 35 U.S.C. 102(b):

Applicant argues:

> The semiconductor device of claim 6 includes in combination among other features a protective layer "formed directly on said field oxide to prevent overetching of said field oxide, said protective layer being a conductive layer, and being formed so as not to be on edges of said

> field oxide and as having substantially **uniform thickness**". Applicant respectfully submits that the Yoo et al. reference as relied upon does not disclose these features.

First of all, the uniform thickness of the claimed protective layer is **unsupported new matter**.

For the uniform thickness of the protective layer 21 of Yoo, although not explicitly disclosed, it is well known in the art that the thickness of the polysilicon layer should be uniform to ensure the same characteristics of the gate transistors, thus the polysilicon portions that form the protective layer 21 also uniform in thickness, or the same thickness as that of portions 16. Unlike the claimed protective layer, the portions 21 were not being planarized, the thickness of portion 21 is truly uniform in thickness.

Applicant further adds:

> This should be clear, because the Yoo et al. reference does not disclose or suggest **flattening floating gate layer 21 so as to have substantially uniform thickness.**

The above assertion clearly shows that the Applicant could not distinguish between "uniform thickness" and "planar surface". Since planarize the top surface only results in flattening the top surface. In the instant case, as shown in the illustration above, planarizing the top surface of the polysilicon layer on a field oxide (LOCOS) only results in flattening surface, not uniform thickness.

With respect to claims 11 and 16, Applicant repeat the same arguments as that of claim 6. therefore, the same response is applied.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER